DRAM WITH VERY SHALLOW TRENCH ISOLATION

FIELD THE OF INVENTION

[0001] The present invention relates to dynamic random access memory (DRAM) structures, in particular, to vertical DRAM structures.

BACKGROUND OF THE INVENTION

[0002] With the constant drive towards increasing both the operating speeds and capacity of DRAM devices, advances in DRAM technology are directed at reductions in device minimum feature size (F) and achieving more compact cell layouts through reduced device footprint. Reduction in scale of planar DRAM devices is limited by stringent leakage requirements, however. A reduction in gate poly length requires thinner gate oxides, while the reduction in gate poly length (i.e., channel length) requires increased channel doping to avoid short channel effects. High doping levels, on the other hand, increase junction leakage which, in turn, decreases data retention time. These and other challenges surrounding the scaling of planar DRAM devices have provided the motivation for vertical transistors. These devices introduce both additional degrees of freedom as well as constraints in the design of conventional planar devices.

[0003] The design of the resulting vertical devices has involved an asymmetric cell structure, in which the transistor and the corresponding buried strap (e.g., one-sided strap or "OSS") are formed along the upper region of a trench capacitor. The OSS lies along one vertical edge of the cell device between the transistor and capacitor. However, positioning multiple devices in close physical proximity to one another introduces a potential for electrical cross-talk between cells, entailing defective operation of the devices. This risk has been mitigated by introducing shallow trench isolation ("STI"), which provides lateral isolation

between adjacent cells. The STI may extend approximately 200-400 nm below the buried strap.

[0004] This resulting configuration, while theoretically advantageous, suffers from manufacturing difficulties that are related to the fabricated STI. As the feature size of the vertical DRAM device decreases, the resulting aspect ratio of the device, defined as depth of trench divided by trench separation, increases. This makes the device difficult to form using known processes without the formation of unacceptable voids and other defects. In essence, the resulting increase in aspect ratio of a trench, which can fall in the range of 4-8, may turn out to be difficult to fill properly with oxide. Though intended to neatly fill it from the bottom, as the oxide is deposited into the space allocated for the formation of the STI it tends also to grow at the side walls. This growth can occur to such an extent that the resulting side wall formations actually touch, forming a structure having a shape reminiscent of that of a bishop's mitre. This undesired structure interrupts the downward flow of oxide, leading to the formation of undesirable voids. In addition to being unpredictable, the voids undermine the electrical characteristics of the STI and defeat its purpose.

[0005] Accordingly, there is a need for a solution to the problems associated with forming STI as the device minimum feature size (F) shrinks. Moreover, there is a need to form STI using a practical approach to the manufacture of vertical DRAMs.

SUMMARY OF THE INVENTION

[0006] The present invention solves at least in part the long felt, but unmet, needs described above. In particular, the methods and structures of the present invention involve the recognition that the buried strap of a vertical DRAM structure can be laterally constrained, thereby maintaining freedom from cross talk in the absence of an adjacent STI, even at 6F2 scaling (where F2 is the square of the minimum feature size and 6F2 is the minimum size of a unit cell

having a transistor and storage node, i.e., the 6F2 unit cell area is six times the minimum feature size area). The methods and structures of the present invention involve the further recognition that the STI can therefore be vertically confined, freed of any need to extend down below the level of the buried strap. The reduction of the buried strap to 1F width and the concomitant reduction in the depth of the STI together permit a significantly reduced aspect ratio, in turn enabling critically improved manufacturability and resulting in an integration scheme capable of allowing scalability of the 6F2 cell to 60 nm ground rules.

[0007] An aspect of the present invention provides a vertical dynamic random access memory (DRAM) cell device fabricated within a trench region in a substrate, the trench having first and second opposing substantially vertical edges. The vertical DRAM cell comprises a storage capacitor formed within the trench region for storing electrical charge, a transistor formed within the trench region above the storage capacitor, and a buried strap formed on the first vertical edge between the storage capacitor and the transistor, wherein the buried strap electrically couples the storage capacitor and the transistor. An isolation collar region is formed on the second vertical edge of the trench, such that the isolation collar extends the length of the transistor. The isolation collar has a bottom edge that is vertically separated from the top surface of the buried strap by about 500 to 1000 nm.

[0008] Another aspect of the present invention provides a buried strap for electrically connecting a transistor and a storage capacitor in a vertical dynamic random access memory (DRAM) cell device formed within a semiconductor substrate, wherein the DRAM cell comprises a trench having a first and a second opposing vertical edge, where the buried strap comprises: an electrically conducting region formed within the trench, wherein the electrically conducting region is formed proximate to the first opposing edge between the transistor and storage capacitor, and laterally displaced from an isolation region formed on the second opposing vertical edge. The isolation region extends from the

semiconductor substrate surface along the second opposing vertical edge and terminates no lower than the electrically conductible region.

[0009] Yet another aspect of the present invention provides shallow trench isolation in a vertical dynamic random access memory (DRAM) cell device having a storage capacitor and a transistor formed in a trench region. The trench region has a first edge, a second edge, and a trench bottom, whereby the trench extends vertically downwards from a semiconductor substrate surface to the trench bottom. The method comprises: isolating a region adjacent to the first edge of the trench, where the isolated region extends vertically downwards from the semiconductor substrate surface in the direction of the trench bottom to a depth, wherein the region is isolated from at least one DRAM cell device which is proximate to the first edge. The method further comprises connecting the storage capacitor to the transistor at a connection location adjacent to the second edge of the trench, whereby the connection location is laterally displaced from the isolated region adjacent to the first edge. The isolated region terminates no lower than the connection location adjacent to the second edge.

[0010] Another aspect of the present invention provides a method of fabricating an isolation region for shallow trench isolation in a vertical dynamic random access memory (DRAM) cell device having a transistor and a capacitor formed in a trench, the trench having a first edge and an opposing second edge, whereby the method comprises: lining the first edge and opposing second edge of the trench with an oxide material and partially filling the trench with polysilicon, wherein the polysilicon has a top surface. The oxide material lining is removed from the first edge of the trench and a divot is formed in the surface of the polysilicon proximate to the first edge of the trench. The divot in the polysilicon is then filled with an electrically conductive material, whereby the electrically conductive material forms a buried strap.

[0011] An aspect of the present invention further provides a vertical dynamic random access memory (DRAM) device comprising: a plurality of cell devices,

where each of the plurality of cell devices comprises a trench having a trench depth and substantially vertical opposing edges. The respective vertical opposing edges of an adjacent pair of the plurality of cell devices are separated by a separation width, whereby the ratio between the trench depth and the separation width between the adjacent pair of cell devices comprises a value of less than about 1.5.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figure 1A illustrates a top plan view of a portion of an embodiment of DRAM memory device in accordance with the present invention, in which four vertical DRAM cell footprints are shown.

[0013] Figure 1B illustrates a cross sectional view along the A-A' axis of FIG. 1A, which shows the trench regions of the vertical DRAM cells.

[0014] Figure 2A illustrates another top plan view of a portion of the DRAM memory device in accordance with the present invention, where silicon nitride is selectively deposited on the device surface.

[0015] Figure 2B illustrates a cross sectional view along the A-A' axis of FIG. 2A, which shows the deposited polysilicon layer within the trench regions.

[0016] Figure 3 illustrates a cross sectional view of the trench regions, where oxide is deposited within the trench regions.

[0017] Figure 4 illustrates a cross sectional view of the trench region, where polysilicon is deposited over the deposited oxide.

[0018] Figure 5A illustrates another top plan view of a portion of the DRAM memory device in accordance with the present invention, where the device surface is patterned with an etch resist.

[0019] Figure 5B illustrates a cross sectional view along the A-A' axis of FIG. 5A.

[0020] Figure 6A illustrates a top plan view of a portion of the DRAM memory device in accordance with the present invention, where areas not covered by the resist are etched.

[0021] Figure 6B illustrates a cross sectional view along the A-A' axis of FIG. 6A, where polysilicon is etched from within the trench regions.

[0022] Figure 7A illustrates a top plan view of a portion of the DRAM memory device in accordance with the present invention, where oxide is deposited within the trench.

[0023] Figure 7B illustrates a cross sectional view along the A-A' axis of FIG. 7A, where an oxide lining is deposited on the trench walls.

[0024] Figure 8A illustrates a top plan view of the DRAM memory device, where an etch resist material is deposited within the trench.

[0025] Figure 8B illustrates a cross sectional view along the A-A' axis of FIG. 8A, where the etch resist fills the trench region.

[0026] Figure 9A illustrates a top plan view of the DRAM memory device, where an oxide and silicon nitride layer are etched from the surface.

[0027] Figure 9B illustrates a cross sectional view along the A-A' axis of FIG. 9A, where both the oxide and silicon nitride layer are etched from the surface of the device.

[0028] Figure 9C illustrates a cross sectional view along the B-B' axis of FIG. 9A, where the oxide layer is etched from the surface of the device.

[0029] Figure 10A illustrates a vertical opening within the etch resist-filled trench shown in FIG. 9C.

[0030] Figure 10B illustrates the removal of a portion of collar oxide from the vertical edge of the trench.

[0031] Figure 10C illustrates the formation of a divot in the collar oxide region.

[0032] Figure 10D illustrates deposited polysilicon for filling the divot and producing a buried strap.

[0033] Figure 10E illustrates removing excess polysilicon from the walls of the trench following the divot fill process shown in FIG. 10D.

[0034] Figure 10F illustrates the removal of the silicon nitride lining from the collar regions.

[0035] Figure 11A illustrates a top plan view of the DRAM memory device, where an oxide is deposited to form a Trench top oxide.

[0036] Figure 11B illustrates a cross sectional view along the A-A' axis of FIG. 11A, where oxide is deposited within the trench recess and the device surface.

[0037] Figure 11C illustrates a cross sectional view along the B-B' axis of FIG. 11A, where oxide is deposited within the trench recess and the device surface.

[0038] Figure 12A illustrates a cross sectional top plan view of the DRAM memory device, where polysilicon is deposited within the trench and over the device surface.

[0039] Figure 12B illustrates a cross sectional view along the A-A' axis of FIG. 12A, where polysilicon fills the trench and covers the surface oxide.

[0040] Figure 12C illustrates a cross sectional view along the B-B' axis of FIG. 12A, where polysilicon fills the trench and covers the surface oxide.

[0041] Figure 13A illustrates a cross sectional view along the A-A' axis of FIG. 12A, where chemical mechanical polishing (CMP) is applied to the polysilicon and oxide surfaces.

[0042] Figure 13B illustrates a cross sectional view along the B-B' axis of FIG. 12A, where Chemical Mechanical Polishing (CMP) removes the polysilicon layer on the surface of the device.

[0043] Figure 14A illustrates a top plan view of the device, where the separation between vertical DRAM cells is shown.

[0044] Figure 14B illustrates a top plan view of the device, where the trench depth of a vertical DRAM cell is shown.

DETAILED DESCRIPTION

[0045] Figure 1A illustrates a top view of four vertical DRAM cell footprints 10 corresponding to four vertical DRAM cells during fabrication of a shallow trench isolation (STI) region in an embodiment of the present invention. The four vertical DRAM cells are depicted for purposes of illustration only. A typical DRAM device will typically incorporate a large number of cell devices having different layout or footprint arrangements. Each footprint 10 includes a doped polysilicon pad 12 and a collar oxide region (which can also be referred to more generally as an isolation collar) 14, the collar oxide 14 forming the perimeter of pad 12.

[0046] Figure 1B shows a cross sectional view along A-A' of the structure shown in Figure 1A. As illustrated in the figure, each doped polysilicon pad 12 (Figure 1A) corresponds to a vertical trench 22 extending from the device surface into semiconductor substrate region 20. Each vertical trench 22 has been filled with doped polysilicon, as indicated by polysilicon regions 18. Also, as illustrated in Figures 1A and 1B, undoped polysilicon surface 16 surrounds collar oxide regions 14 and pads 12. The collar oxide 14 is an integral part of vertical DRAM cell fabrication in that it prevents electrical discharge of the capacitor due to an uncontrolled parasitic transistor leading to an unwanted electric current path within the DRAM cell.

[0047] As illustrated in Figure 2A, conventional masking or lithography techniques are used to deposit a layer of silicon nitride 24 onto undoped polysilicon surface 16 (Figure 1A). The silicon nitride layer 24 is deposited on both undoped polysilicon surface 16 (Figure 1A) and collar oxide regions 14. Only the doped polysilicon pads 12 (Figure 1A) are not covered with the deposited silicon nitride 12. As shown in Figure 2B, polysilicon regions 18

(Figure 1B) are etched down to a depth of between approximately 200-400 nm to form a recess 26 within each trench region 22.

[0048] As illustrated in Figure 3, following the etching of polysilicon regions 18, an oxide pad layer 30 is deposited within recess regions 26 onto surface 23 of the remaining polysilicon. A silicon nitride liner 32 is then deposited over the inner surfaces or walls of recess regions 26. As silicon nitride is deposited, the silicon nitride liner 32 is also deposited over silicon nitride layer 24.

[0049] As illustrated in Figure 4, once silicon nitride liner 32 is deposited, undoped polysilicon 36 is filled within recess region 26 and over silicon nitride layer 24. The polysilicon 36 that fills recess 26 also form a layer of polysilicon 37 over the silicon nitride layer 24.

[0050] Figure 5B illustrates step of chemical mechanical polishing (CMP) the deposited undoped polysilicon 36 or other suitable treatment. Following the CMP process, an oxide layer 40 is deposited over the silicon nitride layer 24. The thickness of this layer is approximately 1.5 times the thickness of the silicon nitride layer 24. Figure 5B also further illustrates etch resist mask 42 formed over oxide layer 40, where the mask 42 provides selective etching of regions 44 that are not protected by mask 42. Figure 5A shows a top plan view of Figure 5B, and illustrates etch resist mask 42 and regions 44. Figure 5B is a cross-sectional view along axis A-A' of Figure 5A.

[0051] Figure 6B illustrates the etch process of regions 44 shown in Figures 5A and 5B, in a cross-sectional view of Figure 6A taken along axis A-A'. The undoped polysilicon 36 within recess regions 26 (Figure 5B), and the portion of silicon nitride liner 32 that had been formed on the top surface of oxide pad layer 30 has been etched away. Following the etching, only an undoped polysilicon liner 46 remains deposited on the inner vertical walls of recess regions 26. Silicon nitride layer 24 and oxide layer 40 within regions 44 were also etched.

[0052] The undoped polysilicon liner 46 (Figure 6B) deposited on the inner walls of recess region 26 is oxidized, as illustrated in Figure 7B, a cross sectional view

of Figure 7A taken along axis A-A'. Figure 7B also shows that the etch resist mask 42 is removed.

[0053] Following the formation of oxidized polysilicon liner 50 (Figure 7B), recess regions 26 are filled with an etch resist material 52, as illustrated in Figure 8B. Figure 8B also shows oxide layer 40 and silicon nitride layer 24 that have been deposited on the silicon surface 54 of the semiconductor material used to fabricate the vertical DRAM cells. Figure 8B is a cross-sectional view of Figure 8A taken along axis A-A', where Figure 8A shows a top view of the etch resist material 52. Figure 8B is a cross sectional view of Figure 8A taken along axis A-A'.

[0054] Figure 9B shows the etching of oxide layer 40 and silicon nitride layer 24 down to the silicon surface 54. As shown in the figure, an additional layer of silicon is etched away, taking the silicon surface down to a level indicated at 56. This etching process is carried out in the direction of axis A-A' shown in Figure 9A, where Figure 9B shows a cross sectional view of A-A'. Figure 9C shows a cross sectional view of Figure 9A taken along axis B-B'. As illustrated, oxide layer 40 is etched down to the silicon nitride layer 24.

[0055] As illustrated in Figure 10A, the etch resist material 52 filling recess regions 26 (Figure 7B) is partially etched along vertical edges 60. This creates a vertical channel opening 62 down each of the vertical edges 62. Vertical channel opening 62 allows further etching for generating a buried strap. The buried strap connects the transistor (not shown) and the capacitor (not shown) of a single unit cell to form a DRAM storage node within each trench region 22 (Figure 1B). As shown in Figure 10A, the areas surrounding vertical channel opening 62 that are not covered by etch resist 52 are further etched.

[0056] As illustrated in Figure 10B, the oxidized polysilicon liner 50 (Figure 10A) along vertical edges 60 is etched away, including a partial section of oxide pad layer 30. Figure 10B also shows that a portion of collar oxide 14 (Figure 10A)

along vertical edges 60 is etched. This portion along each vertical edge 60 is defined by 66.

[0057] As shown in Figure 10C, an opening or divot 68 is etched into the upper portion of oxide pad layer 30. Once divot 68 has been formed, an electrically conductive material, such as doped or undoped polysilicon 70, is deposited into recess regions 26, as shown in Figure 10D. As a result of the deposited polysilicon 70, the inner walls of the recess regions 26 are covered by doped or undoped polysilicon 70. Accordingly, divot 68 is also filled with deposited doped or undoped polysilicon 70.

[0058] As illustrated in Figure 10E, the polysilicon filled divot then forms a buried strap 72. Figure 10E further illustrates the removal of excess deposited polysilicon 70 from the inner walls with recess regions 26.

[0059] Figure 10F shows collar oxide 14, where the silicon nitride deposited over each collar oxide 14 adjacent to edges 74 is removed. As illustrated, each buried strap 72 is laterally displaced from the opposing oxide collar 14 on vertical edge 74. Each opposing oxide collar 14 forms a Shallow Trench Isolation (STI) region 76 and vertically terminates above buried strap 72 located adjacent vertical edge 60. The strap can be flush with the vertical edge, as shown, or set further in from the edge, provided that its distance from vertical edge 74 is sufficient, e.g., about 50-150 nm in an embodiment of this aspect of the present invention, to isolate buried strap 72 from an adjacent cell proximate to vertical edge 74, as described below. In one embodiment, buried strap 72 has a vertical dimension in the range of about 30 to 150 nm and a lateral dimension in the range of about 50 to 100 nm.

[0060] The shallow trench isolation region 76 provides electrical isolation between adjacent DRAM cells 1 and 2 that have been formed in trench regions 22 (Figure 1). These isolation regions avoid electrical cross talk between the capacitor and transistor devices (not shown) of each adjacent DRAM cell, while buried strap 72 provides electrical connectivity between the capacitor and

transistor devices within each cell. In relation to both vertical DRAM cells 1 and 2 shown in Figure 10F, the capacitor device is formed below the buried strap 72, while the transistor device is formed above the strap 72. The actual transistors and capacitors formed within the trench regions have not been illustrated or described herein as these device and their fabrication are know in the art. As shown in Figure 10F, region 80 is where a transistor is formed, and region 82 is where a capacitor is formed.

[0061] In one embodiment of this aspect of the present invention, the depth of the STI region 76 is less than or equal to about 250 to 350 nm. Even more shallow depths, such as from 50 to 150nm or less, may also be desirable and within the scope of the present invention. STI region 78 provides similar isolation between cell 2 and another adjacent DRAM device (not shown). Within each cell, the lateral displacement of the buried strap 72 with respect to the oxide collar 14 enables the oxide collar 14 to terminate roughly at or above the buried strap 72 in the vertical direction, which allows for a shorter depth of isolation and thus a shallower trench. In one embodiment of this aspect of the present invention, the collar oxide 14 has a bottom edge extending below the vertical location of the top surface of the buried strap by about 50-100 nm and vertically separate from the top surface of the buried strap by about 500-1000 nm.

[0062] Once the buried strap 72 is formed, a trench top oxide (TTO) layer 86 is deposited over oxide pad layer 30, as shown in Figure 11B. As illustrated, this oxide deposition process produces an oxide layer 88 on the silicon surface 54 of the semiconductor material used to fabricate the vertical DRAM cells. Figure 11B is a cross sectional view of Figure 11A taken along axis A-A' (major axis of trench), whereas Figure 11C is a cross sectional view of Figure 11A taken along axis B-B' (minor axis of trench). As illustrated in Figure 11C, the oxide deposition process produces an oxide layer 90 over silicon nitride layer 24 as well. In one embodiment of this aspect of the present invention, the top portion of the buried strap 72 may vertically separated from the bottom surface of the TTO layer 86 by about 150 to 450 nm.

[0063] The TTO layer 86 isolates the gate (not shown) of the transistor formed in region 80, from the capacitor formed in region 82. Therefore, as shown in Figure 11C, the electrical connection between the transistor drain or source and the capacitor is provided through buried strap 72. Applying appropriate voltage to the gate generates a low channel resistance between the drain and source of the transistor, thus allowing the capacitor to charge or discharge through the low resistance channel, which electrically connects the capacitor to a bitline (not shown).

[0064] Region 80 of the trench, in which the transistor is partly formed, is filled with polysilicon as shown in Figures 12B and 12C. As shown in both Figure 12B and 12C, polysilicon filler 90 is deposited over TTO layer 86, filling the trench completely, and covering oxide layer 88. Figure 12B is a cross sectional view of Figure 12A taken along axis A-A' (major axis of trench), and Figure 12C is a cross sectional view of Figure 12A taken along axis B-B' (minor axis of trench). Chemical Mechanical Polishing (CMP) is then applied to the surface 92 of the polysilicon filler 90, as shown in Figures 12B and 12C.

[0065] The effect of the CMP process in planarizing surface 92 is illustrated in Figure 13A and 13B. As illustrated in the cross sectional view along the B-B' axis (Figure 13B), the layers of polysilicon filler 90 (Figure 12C) deposited on top of oxide layer 88 (Figure 12C), and the oxide layer 88 (Figure 12C) are polished down to silicon nitride layer 24. As illustrated in Figure 13A, following the CMP process, the polysilicon filler 90 is polished down to the top surface of oxide layer 88. Using know conventional techniques, word and bit line connections are applied to each Vertical cell DRAM device, such as cell device 96 illustrated in Figure 13A and 13B.

[0066] Figure 14A shows the separation "W" (width) between adjacent DRAM cells 100 and 102, or cells 104 and 106, where Figure 14B illustrates the depth "d" of a trench corresponding to cells 100, 102, 104, or 106. The Aspect Ratio (AR) of a DRAM device is defined as the ratio of depth "d" to separation 'W" (i.e.,

d/W). As the device densities increase, "W," becomes smaller, leading to higher aspect ratios. Thus, to accommodate the higher densities, the trenches become narrower, which may lead to some fabrication difficulties. For example, when depositing oxide within the trench and on the trench walls, the high aspect ratio may cause the deposited material to grow in the shape of a bishop's miter, which may interrupt the material flow and generate a void that may result in operational deficiencies. In accordance with the present invention, the STI region allows for a reduction in trench depth "d," which leads to a lower AR. By having a lower AR, higher density vertical DRAM devices can be produced without encountering fabrication and manufacturing obstacles of the sort described in the Background section, above.

[0067] Figure 15 shows a top plan view of a bitline 110 that connects to a series of DRAM cells, such as cells 112 and 114. As illustrated each cell connects to bitline 110 via borderless contacts 116. Charging and discharging of the storage capacitor within each cell is via a borderless contact such as borderless contact 116, and a bitline, such as bitline 110.

[0068] Figure 16 shows a cross sectional view of a vertical DRAM cell having both a gate contact 120 and a bitline contact 122. As illustrated, the transistor is formed in region 124 (i.e., upper portion of trench), and the storage capacitor is formed in region 126 (i.e., lower portion of trench), where both the storage capacitor and transistor are connected by buried strap 128. To switch the transistor "ON," an appropriate voltage or electrical signal is applied to gate contact 120 via a wordline (not shown), which is part of the DRAM array architecture. The gate voltage generates the necessary electric field for driving the transistor into saturation along oxide collar region 130. Once the transistor is "ON," electrical storage charge is coupled via the bitline 110 (Figure 15) to the bitline contact 122, and through the transistor channel (i.e., between drain and source) to the storage capacitor formed in region 126.

[0069] In addition to the embodiments of the aspects of the present invention described above, those of skill in the art will be able to arrive at a variety of other arrangements and steps which, if not explicitly described in this document, nevertheless embody the principles of the invention and fall within the scope of the appended claims. For example, the ordering of method steps is not necessarily fixed, but may be capable of being modified without departing from the scope and spirit of the present invention.